

AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 1, as follows:

BACKGROUND OF THE INVENTION

Please amend the paragraph beginning at page 1, line 2, deleting the underline as follows:

~~Field of the Invention~~ **FIELD OF THE INVENTION**

Please amend the paragraph beginning at page 1, line 7, as follows:

~~Description of the Prior Art~~ **BACKGROUND**

Please amend the paragraph beginning at page 1, line 12, as follows:

Tracing the activity of a data processing system whereby a trace stream is generated including data representing the step-by-step activity within the system is a highly useful tool in system development. However, with the general move towards more deeply embedded processor cores, it becomes more difficult to track the state of the processor core via externally accessible pins. Accordingly, ~~as well as~~ off-chip tracing mechanisms for capturing and ~~analysing~~ analyzing trace data, ~~and~~ increased amounts of tracing functionality are being placed on-chip. Examples of such on-chip tracing mechanisms are the Embedded Trace Macrocell provided by ARM Limited, Cambridge, England in association with their ARM7 and ARM9 processors. Such tracing mechanisms produce in real time a trace stream of data representing activities of the data processing system that are desired to be traced. This trace stream can then subsequently be used to facilitate debugging of sequences of processing instructions being executed by the data processing system.

Please amend the paragraph beginning at page 3, line 1, as follows:

SUMMARY OF THE INVENTION

Please amend the paragraph beginning at page 8, line 11, deleting the underlining as follows:

~~BRIEF DESCRIPTION OF THE DRAWINGS~~

BRIEF DESCRIPTION OF THE DRAWINGS

Please amend the paragraph beginning at page 9, line 9, as follows:

~~DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT~~

Please amend the paragraph beginning at page 16, line 10, as follows:

This problem can be avoided by employing the additional circuitry 630 illustrated in Figure 9 in association with any CID comparator 600 which may generate match signals directly, i.e. without any further qualification by address. Accordingly, the output from the CID comparator 600 is input to an AND gate 620 which receives as its other input the output of NAND gate 610. This NAND gate 610 is arranged to receive three signals, which indicate whether the processor core is operating in privileged mode, whether software debug is enabled, and identify when no further address comparison is being used to qualify the output of CID comparator 600. As long as one of the three signals is not activated, NAND gate 610 will output a logic one value, which will enable the match signal generated by the CID comparator 600 to be output directly as a match signal. However, if all three signals are at a logic one level, i.e. the processor core is operating in privileged mode, software debug is enabled, and no further address comparison is being used, then NAND gate 610 will output a logic zero value, which will prevent the output from CID comparator 600 from being issued until such time as one of the three inputs to the NAND gate is de-asserted. The manner in which this circuitry assists in avoiding the problem illustrated in Figure 8A can be seen when considering Figure 8B.